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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,396	12/10/2003	Ching-Nan Hsiao	NTCP0020USA	1395

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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,396	HSIAO ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,15 and 16* is/are rejected.

7)☒ Claim(s) *13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7-11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer, US patent No. 6,747,306 in view of Arnold, US patent No. 5,937,296.

Regarding claim 1, Dyer teaches (fig. 1) a vertical dynamic random access memory (DRAM, col. 2, lines 66-67) comprising: a substrate (104) comprising at least a deep trench (102) having an upper trench portion (region where element 114 is formed) and a lower trench portion (region where element 106 is formed); a trench capacitor (not shown, col. 3, lines 1-10) located in the lower trench portion; a source-isolation oxide layer (112, referred here trench top oxide) located on the trench capacitor (fig. 1) and an STI (124); and a vertical transistor (col. 3, lines 10-13) located on the source-isolation oxide layer (112), the vertical transistor comprising: an annular source (120) set in the substrate next to the source-isolation oxide layer (112), the annular source being electrically connected to the trench capacitor (fig. 1, via the cell node); a gate conductive layer (114) filling the upper trench portion; a cylindrical gate dielectric layer (116) located on a surface of a sidewall of the upper trench portion and circularly encompassing the gate conductive layer (114); and an annular drain (118) circularly

encompassing the deep trench near a surface of the substrate (104), the annular drain being positioned next to the STI (124) and electrically connected to a second contact plug (134).

Dyer does not explicitly teach that the shallow trench isolation (STI) is positioned around the deep trench or the STI is completely compassing the vertical transistor and separating the annular drain from other annular drains of any adjacent vertical transistor in the substrate.

Arnold teaches (fig. 1) STI structure (18) completely compassing the active surface region of the memory cell structure (11) and separating the memory cell structure from any adjacent memory cell in the substrate (fig. 1 and col., 6, lines 26-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the STI structures taught by Arnold in the structure of Dyer in order to provide better isolation. The modified structure of Dyer and Arnold would have an STI structure, where the STI completely compassing the vertical transistor and separating the annular drain from other annular drains of any adjacent vertical transistor in the substrate.

Regarding claim 2, Dyer teaches substantially the entire claimed structure of claim 1 above including a storage node filling (not shown) the lower trench portion and electrically connected to the annular source (120); a capacitor dielectric layer (inherent property of storage capacitor) encompassing the storage node; and a buried plate (not shown) located in the substrate in a side of the capacitor dielectric layer (refer to col. 3, lines 4-10).

Regarding claim 3, Dyer teaches (fig. 1) substantially the entire claimed structure of claim 1 above including the buried plate (col. 3, lines 4-5) surrounds a sidewall of the lower trench portion (inherent structure of buried plate), and the capacitor dielectric layer (not shown) is located on a surface of the sidewall of the lower trench portion so as to isolate the storage node and the buried plate (inherent structure of trench capacitor and refer to col. 3, lines 1-10 and fig. 1).

Regarding 4, Dyer teaches (fig. 1) substantially the entire claimed structure of claim 1 above including the trench capacitor further comprises a buried strap (110) for electrically connecting the annular source and the storage node (fig. 1 and col. 3, lines).

Regarding claim 5, Dyer teaches (fig. 1) substantially the entire claimed structure of claim 1 above including the buried strap (110) is an annular conductive strap located on the surface of the sidewall of the lower trench portion above the capacitor dielectric layer (not shown).

Regarding claim 7, Dyer teaches (fig. 1) substantially the entire claimed structure of claim 1 above including the annular source (120) is an ion diffusion area (col. 3, line 19).

Regarding claim 8, Dyer teaches (fig. 1) substantially the entire claimed structure of claim 1 above including the annular drain (118) is a heavily doped area.

The limitation that annular drain overlaps ion implantation area is not given patentable weight, because it is product by process claim. "[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its

method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claim 9, Dyer teaches substantially the entire claimed structure of claim 1 above including a passivation layer (132) covering the surface of the substrate and the transistor.

Regarding claim 10, Dyer teaches (fig. 1) substantially the entire claimed structure of claim 1 above including the first and the second contact plug are electrically connected to a word line and a bit line respectively (portion of the 122 and 134 could serve as word line contact and bit line contact respectively).

Regarding claim 11, Dyer teaches substantially the entire claimed structure of claim 1 above the STI surrounds the annular source and the annular drain region without overlapping the deep trench (figs. 1 of Arnold).

Regarding claim 16, Dyer teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the annular drain positioned below the second contact plug having a larger width from the STI to the deep trench than a width of a portion of the annular drain not positioned below the second contact plug.

Parameters such as thickness and width in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the width of the annular drain as claimed in order to make appropriate contact for further integration.

3. Claims 6, 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dyer, Arnold and in further view of Radens et al., US patent No. 6,437,388.

Regarding claim 6, Dyer teaches substantially the entire claimed structure of claim 1 above except explicitly stating that conductive layer is located on the gate conductive layer for electrically connecting the gate conductive layer and the first contact plug.

It is conventional in the art to form a silicide structure on top of gate layers to reduce the contact resistance between the gate structure and contact plugs. Radens also teaches (fig. 11) forming a conductive layer (72) such as tungsten silicide on top of the gate structure (28) in order to form a contact with improved conductivity.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive layer taught by Radens on the gate conductive layer of Dyer in order to reduce the contact resistance between the gate and the contact plug that is subsequently formed.

Regarding claim 12, Dyer teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the annular spacer surrounding the entire upper trench portion.

It is conventional and also taught by Radens (figs. 4-5 and 13) where an annular spacer structure (36) that is formed surrounding the entire upper trench portion.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the spacer structure taught by Radens in the structure of Dyer in order to protect the gate conductor from shorting.

Regarding claim 15, Dyer teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the annular spacer positioned on an outer surface of the sidewall of the entire upper trench portion.

It is conventional and also taught by Radens (figs. 4-5 and 13) where a spacer structure (36) that is formed on an outer surface sidewall of upper trench (trench where 28 is formed).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the spacer structure taught by Radens in the structure of Dyer in order to protect the gate conductor from shorting.

Allowable Subject Matter

4. Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reason for indicating Allowable Subject Matter

5. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach or suggest, singularly or in combination at least the limitation of " the second contact plug has an asymmetric structure, which is

positioned on the spacer and the drain while contacts the spacer and the drain at the same time" as recited in claim 13.

The prior art of record does not teach or suggest, singularly or in combination at least the limitation of "wherein the second contact plug is positioned above a portion of the STI and directly contacts the STI and the annular spacer near the STI at the same time" as recited in claim 14.

Response to Arguments

6. Applicant's arguments with respect to claims 1-13 and 15-16 have been considered but they are moot in view of new grounds of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
March 3, 2006

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